1ppm DAC
20-Bit, ±1LSB INL,Voltage Output DAC

Preliminary Technical Data

AD5791

FEATURES

1-ppm Resolution
1-ppm INL
9nV/√Hz Noise Spectral Density
1-ppm Output Drift
0.05-ppm/°C Temperature Drift
1µs Settling Time
Glitch Energy 0.4nV-s (5V), 1nV-s (10V)
Operating temperature range: -40°C to 125°C
20-Lead TSSOP and 4x5mm LFCSP Packages
Wide Power Supply Range up to ±16.5V
50 MHz Schmitt Triggered Digital Interface

APPLICATIONS

Medical Instrumentation
Test and Measurement
Industrial Control
High end Scientific and Aerospace Instrumentation

FUNCTIONAL BLOCK DIAGRAM

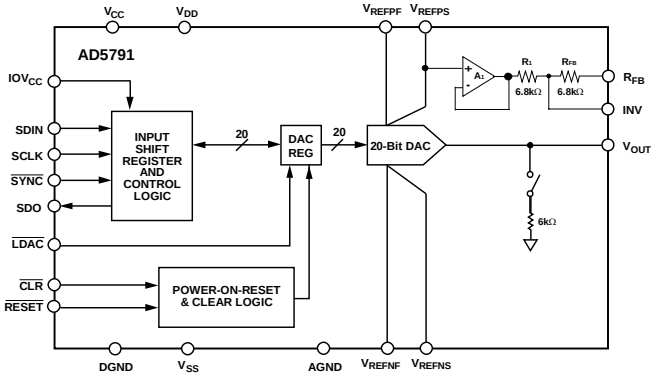

Figure 1.

Table 1. Complementary Devices

Part No.	Description
AD8675	Ultra Precision, 36 V, 2.8 nV/√Hz Rail-to-Rail Output Op Amp
AD8676	Ultra Precision, 36 V, 2.8 nV/√Hz Dual Rail-to-Rail Output Op Amp
ADA4004	1.8nV/√Hz, 36 V Precision Amplifier
ADA4898-1	High Voltage, Low Noise, Low Distortion, Unity Gain Stable, High Speed Op Amp

GENERAL DESCRIPTION

The AD5791 is a single 20-bit, unbuffered voltage-output DAC that operates from a bipolar supply of up to 33V. The AD5791 accepts a positive reference input in the range 4V to V_{DD} – 2.5V and a negative reference input in the range V_{SS} + 2.5 V to 0V. The AD5791 offers a relative accuracy specification of ±1 LSB max, and operation is guaranteed monotonic with a ±1 LSB DNL max specification.

The part uses a versatile 3-wire serial interface that operates at clock rates up to 50 MHz and that is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The part incorporates a power-on reset circuit that ensures the DAC output powers up to 0V and in a known output impedance state and remains in this state until a valid write to the device takes place. The part provides a disable feature that places the output in a defined load state

PRODUCT HIGHLIGHTS

Wide Power supply range up to ±16.5V

High Speed interface with clock speeds up to 50 MHz

Operating temperature Range: -40°C to 125°C

Rev. PrG

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REVISION HISTORY

PrG – Preliminary Version, March 3, 2010

SPECIFICATIONS

V_{DD} = 12.5 V to 16.5 V, V_{SS} = -16.5V to -12.5, V_{REFP} = 10 V, V_{REFN} = -10 V, V_{CC} = 2.7V to 5.5V, R_L = unloaded, C_L = unloaded; T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	A,B Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE					
Resolution	20			Bits	
Relative Accuracy (INL Error)[2]	-1	±0.5	1	LSB	B Version
	-4	±2	4	LSB	A Version
Total Unadjusted Error (TUE)[2]	-4	±2	4	LSB	B Version
	-3	±1.5	3	LSB	T_A = 25°C, B Version
	-7	±4	7	LSB	A Version
	-5	±2	5	LSB	T_A = 25°C, A Version
Differential Nonlinearity (DNL)[2]	-1		1	LSB	Guaranteed monotonic
Full-Scale Error	-3		3	LSB	
	-2	±1	2	LSB	T_A = 25°C
Full-Scale Error Temperature Coefficient	-0.5	±0.05	0.5	ppm FSR/°C	
Zero-Scale Error	-2		2	LSB	
	-1	±0.5	1	LSB	T_A = 25°C
Zero-Scale Error Temperature Coefficient	-0.5	±0.05	0.5	ppm FSR/°C	
Gain Error	-3		3	ppm FSR	
	-2	±1	2	ppm FSR	T_A = 25°C
Gain Error Temperature Coefficient	-0.5	±0.05	0.5	ppm FSR/°C	
Mid-Scale Error	-3		3	LSB	
	-2	±1	2	LSB	T_A = 25°C
Mid-Scale Error Temperature Coefficient	-0.5	±0.05	0.5	ppm FSR/°C	
R1, R_{FB} Matching		0.6		%	
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	V_{REFN}		V_{REFP}	V	
Output temperature Coefficient	-0.5	±0.05	0.5	ppm/°C	Measured at +7.5V output
Output Drift vs. Time		0.1	TBD	ppm	After 1000 hours lifetest at T_A = 125°C
		1	TBD	ppm	After 50 hours, T_A = 25°C
Output Slew Rate		50		V/µs	
Output Voltage Settling Time		0.5	1	µs	¼ scale to ¾ scale code transition
Output Noise Spectral Density		9		nV/√Hz	@ 1 kHz, DAC code = midscale
		9		nV/√Hz	@ 10 kHz, DAC code = midscale
		9		nV/√Hz	@ 100 kHz, DAC code = midscale
Output Voltage Noise		0.6		µV p-p	DAC code = midscale, 0.1 Hz to 10 Hz bandwidth
Digital-to-Analog Glitch Energy					1 LSB change around major carry
		0.4		nV-s	5V output span
		1		nV-s	10V output span
		5		nV-s	20V output span
Digital-to-Analog Glitch Amplitude		TBD		mV pk-pk	
Power-on Glitch Energy		TBD		nV-s	Application of power supplies
Power-on Glitch Amplitude		TBD		mV pk-pk	Application of power supplies
Output Enable Glitch Energy		TBD		nV-s	Output enabled
Output Enable Glitch Amplitude		TBD		mV pk-pk	Output enabled
Digital Feedthrough		0.02		nV-s	
DC Output Impedance (Normal Mode)		3.4		kΩ	

Parameter	A,B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
DC Output Impedance (Output Disabled)		6		kΩ	
Signal-to-Noise Ratio		TBD		dB	
Spurious Free Dynamic Range		TBD		dB	
Total Harmonic Distortion		TBD		dB	
REFERENCE INPUTS					
V_{REFP} Input Range	4		V_{DD} – 2.5V	V	
V_{REFN} Input Range	V_{SS} + 2.5V		0		
Input Current		TBD	TBD	mA	V_{REFP}, V_{REFN}, Code Dependent
DC Input Impedance	TBD	TBD	TBD	kΩ	V_{REFP}, V_{REFN}, Code Dependent
Input Capacitance		TBD		pF	V_{REFP}, V_{REFN}
V_{REFP} Reset Threshold		TBD		V	
LOGIC INPUTS					
Input Current[4]		±1	±2	µA	
Input Low Voltage, V_{IL}			0.3 * IOV_{CC}	V	IOV_{CC} = 1.8 V to 5.5 V
Input High Voltage, V_{IH}	0.7 * IOV_{CC}			V	IOV_{CC} = 1.8 V to 5.5 V
Pin Capacitance		4		pF	
LOGIC OUTPUT (SDO)					
V_{OL}, Output Low Voltage			0.4	V	IOV_{CC} = 1.8V to 5.5V, sinking 1mA
V_{OH}, Output High Voltage	IOV_{CC} – 0.5V				IOV_{CC} = 1.8V to 5.5V, sourcing 1mA
High Impedance Leakage Current			±1	µA	
High Impedance Output Capacitance		5		pF	
POWER REQUIREMENTS					All digital inputs at DGND or IOV_{CC}
V_{DD}	7.5		V_{SS} + 33	V	
V_{SS}	V_{DD} – 33		-2.5	V	
V_{CC}	2.7		5.5	V	
IOV_{CC}	1.8		5.5	V	
I_{DD}		4.2	TBD	mA	
I_{SS}		4.1	TBD	mA	
I_{CC}		800	TBD	µA	
DC Power Supply Rejection Ratio (PSRR)		TBD		dB	ΔV_{DD} ± 10%, V_{SS} = 15V
		TBD		dB	ΔV_{SS} ± 10%, V_{DD} = 15 V
AC Power Supply Rejection Ratio		TBD		dB	ΔV_{DD} = 200mV, 50 Hz/60 Hz, V_{SS} = 15V
		TBD		dB	ΔV_{SS} = 200mV, 50 Hz/60 Hz, V_{DD} = 15 V
Power-Up Time		TBD		µs	

[1] Temperature range : –40°C to +125°C, typical at +25°C.
[2] Performance characterised with AD8676 as reference buffer.
[3] Guaranteed by design and characterization, not production tested.
[4] Total current flowing into all pins.

TIMING CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V, IOV_{CC} = 1.8V to 5.5V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit[1]	Unit	Test Conditions/Comments
t_1[2]	20	ns min	SCLK cycle time
	50	ns min	SCLK cycle time (Readback and daisychain modes)
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge hold time
t_6	10	ns min	Minimum $\overline{SYNC}$ high time
t_7	5	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge ignore
t_8	5	ns min	Data setup time
t_9	5	ns min	Data hold time
t_{10}	10	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ falling edge
t_{11}	TBD	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{12}	20	ns min	$\overline{LDAC}$ pulse width low
t_{13}	TBD	ns max	$\overline{LDAC}$ falling edge to output response time
t_{14}	1	µs max	Output settling time
t_{15}	TBD	ns max	$\overline{SYNC}$ rising edge to output response time ($\overline{LDAC}$ tied low)
t_{16}	20	ns min	$\overline{CLR}$ pulse width low
t_{17}	TBD	ns max	$\overline{CLR}$ pulse activation time
t_{18}	5	ns min	$\overline{SYNC}$ falling edge to first SCLK rising edge
t_{19}	10	ns max	$\overline{SYNC}$ rising edge to SDO tristate
	30	ns max	$\overline{SYNC}$ rising edge to SDO tristate (C_L = 50pF)
t_{20}	10	ns max	SCLK rising edge to SDO valid
	30	ns max	SCLK rising edge to SDO valid (C_L = 50pF)
t_{21}	5	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge ignore
t_{22}	20	ns min	$\overline{RESET}$ pulse width low
t_{23}	TBD	ns min	$\overline{RESET}$ pulse activation time

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{CC}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Maximum SCLK frequency is 50 MHz for write mode and 20MHz for readback and daisychain modes.

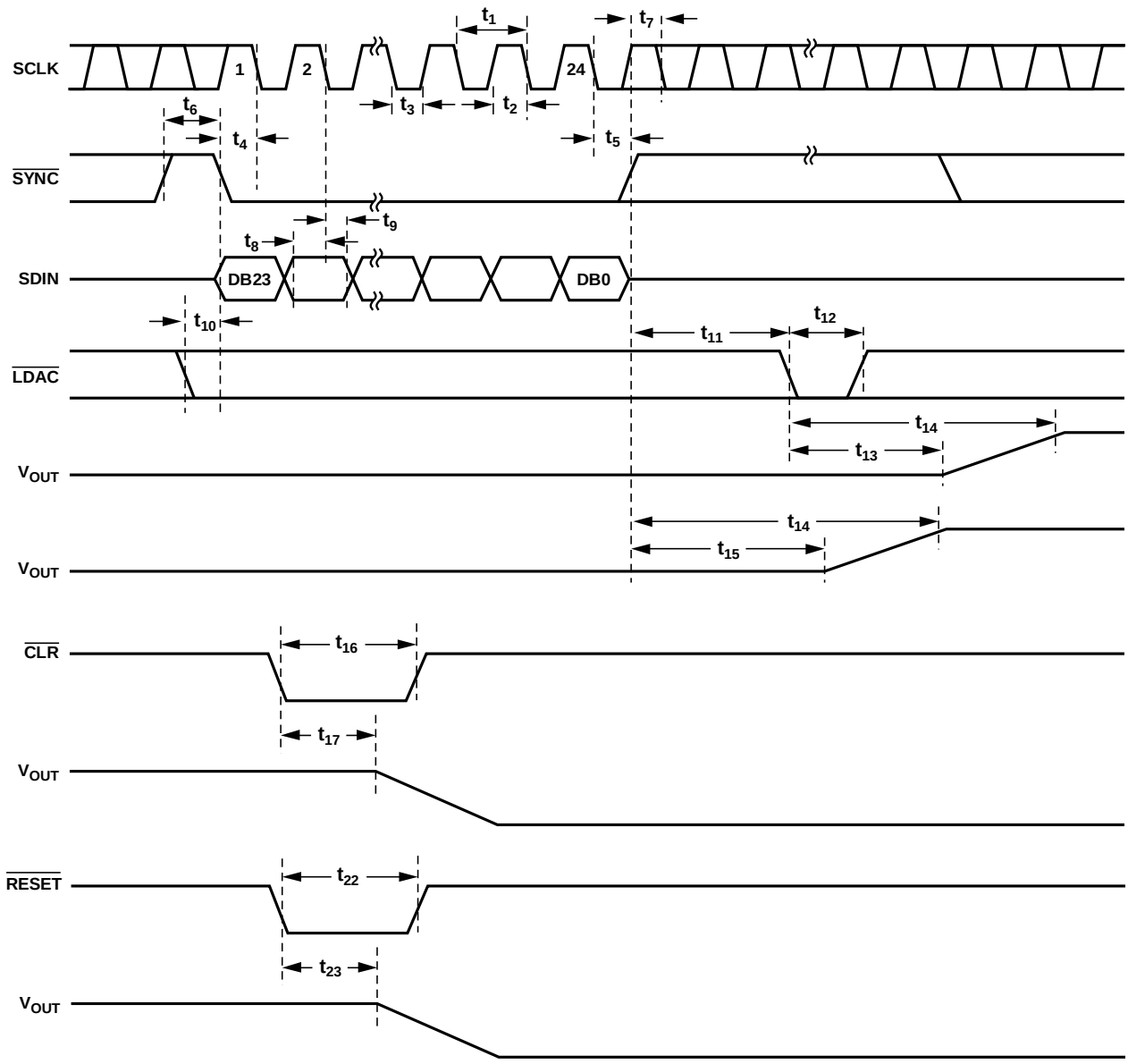

Figure 2. Write Mode Timing Diagram

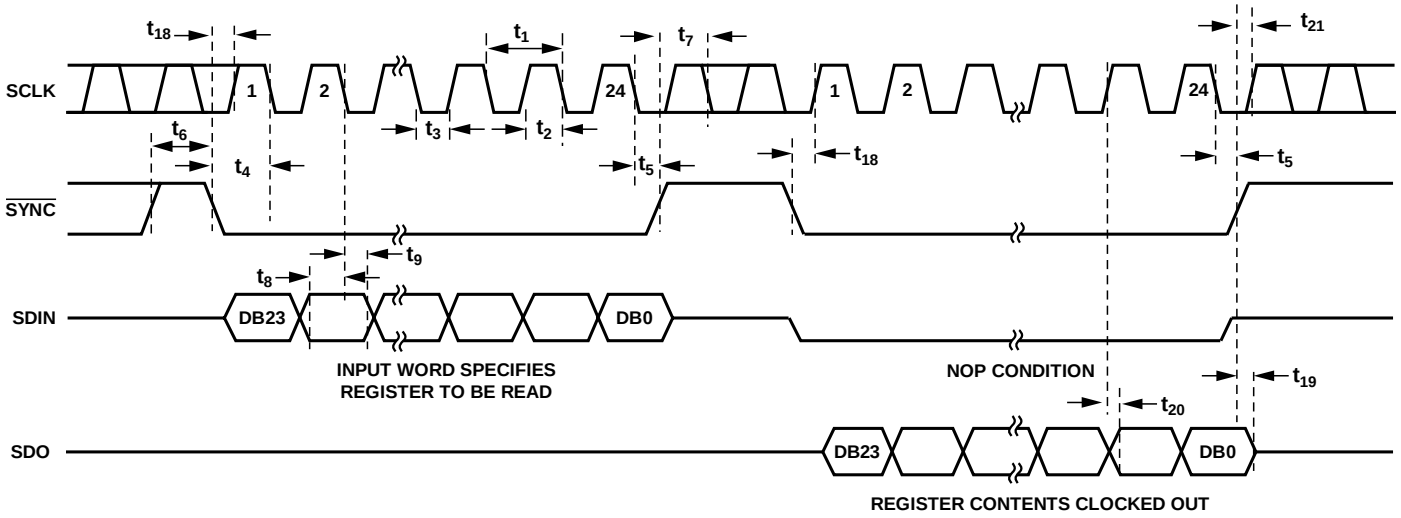

Figure 3. Readback Mode Timing Diagram

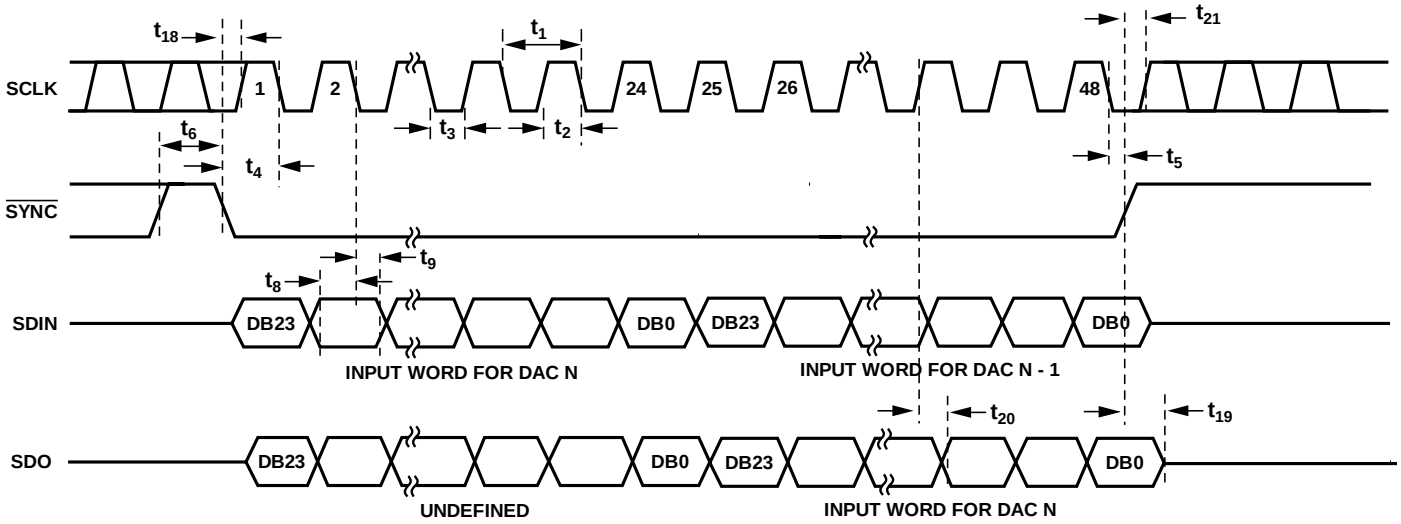

Figure 4. Daisychain Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

TA = 25°C, unless otherwise noted.
Transient currents of up to 100mA do not cause SCR latch-up

Table 4.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +34 V
V_{SS} to AGND	−34V to +0.3V
V_{DD} to V_{SS}	-0.3V to +34V
V_{CC} to DGND	-0.3V to +7V
IOV_{CC} to DGND	-0.3V to +7V
Digital Inputs to DGND (including IOV_{CC})	−0.3 V to DV_{CC} + 0.3 V or +7V (whichever is less)
V_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
V_{REFP} to AGND	−0.3 V to V_{DD} + 0.3 V
V_{REFN} to AGND	V_{SS} − 0.3V to + 0.3 V
DGND to AGND	-0.3V to +0.3V
Operating Temperature Range, T_A	
Industrial	−40°C to + 125°C[1]
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature, T_J max	150°C
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
LFCSP Package	
θ_{JA} Thermal Impedance	TBD°C/W
θ_{JC} Thermal Impedance	TBD°C/W
TSSOP Package	
θ_{JA} Thermal Impedance	TBD°C/W
θ_{JC} Thermal Impedance	TBD°C/W
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020
ESD (Human Body Model)	TBD kV

[1] Temperature range for this device is −40°C to +105°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance integrated circuit with an ESD rating of <TBD kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

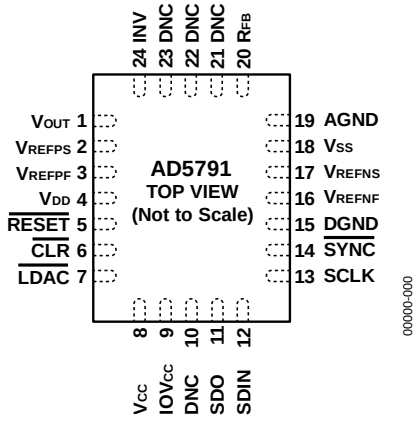

Figure 5. LFCSP pin configuration

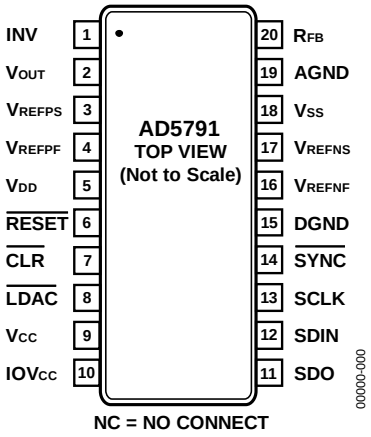

Figure 6. TSSOP pin configuration

Table 5. Pin Function Descriptions

LFCSP Pin No.	TSSOP Pin No.	Mnemonic	Description
1	2	V_{OUT}	Analog output voltage.
2	3	V_{REFPS}	Positive reference sense voltage input. A voltage in the range of 4V to V_{DD} – 2.5V can be connected.
3	4	V_{REFPF}	Positive reference force voltage input. A voltage in the range of 4V to V_{DD} – 2.5V can be connected.
10, 21, 22, 23		DNC	Do not connect to these pins
4	5	V_{DD}	Positive analog supply connection. A voltage in the range of 7.5 V to 16.5 V. can be connected V_{DD} should be decoupled to AGND.
5	6	$\overline{RESET}$	Active Low Reset Pin. Asserting this pin will return the AD5791 to its power on status.
6	7	$\overline{CLR}$	Active Low input. Asserting this pin sets the DAC register to a user defined value (See Table 11) and updates the DAC output. The output value will depend on the DAC register coding that is being used, either binary or 2scomplement.
7	8	$\overline{LDAC}$	Active low Load DAC logic input, This is used to update the DAC register and consequently, the analog output. When tied permanently low, the output is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the input register is updated, but the output update is held off until the falling edge of $\overline{LDAC}$. The $\overline{LDAC}$ pin should not be left unconnected.
8	9	V_{CC}	Digital supply pin. Voltage ranges from 2.7V to 5.5V. DV_{CC} should be decoupled to DGND.
9	10	IOV_{CC}	Digital interface supply pin, Digital threshold levels are referenced to the voltage applied to this pin. Voltage ranges from 1.8V to 5.5V
11	11	SDO	Serial data output.
12	12	SDIN	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	13	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
14	14	$\overline{SYNC}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register, and data is then transferred in on the falling edges of the following clocks. The DAC is updated on the rising edge of $\overline{SYNC}$.
15	15	DGND	Ground reference pin for digital circuitry.
16	16	V_{REFNF}	Negative reference force voltage input. A voltage in the range of V_{SS} + 2.5V to 0V can be connected
17	17	V_{REFNS}	Negative reference sense voltage input. A voltage in the range of V_{SS} + 2.5V to 0V can be connected
18	18	V_{SS}	Negative analog supply connection. A voltage in the range of -16.5 V to -2.5 V can be connected. V_{SS} should be decoupled to AGND.
19	19	AGND	Ground Reference Pin for Analog Circuitry.
20	20	R_{FB}	Feedback connection for external amplifier. See Features section for further details
24	1	INV	Inverting input connection for external amplifier. See Features section for further details
EPAD		V_{SS}	Negative analog supply connection. A voltage in the range of -16.5 V to -2.5 V can be connected.

TYPICAL PERFORMANCE CHARACTERISTICS

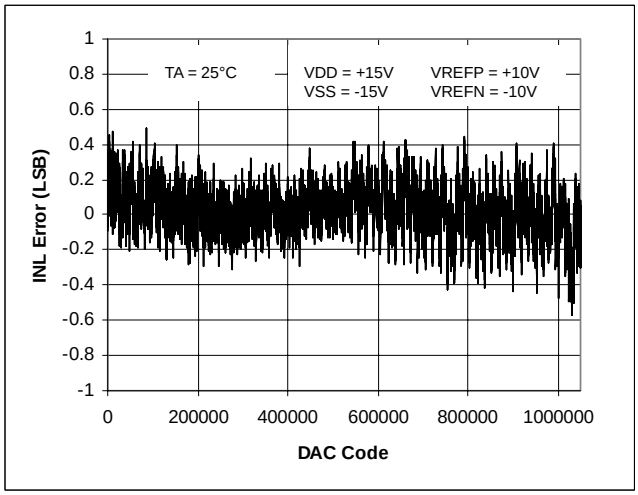

Figure 7. Integral Non Linearity Error vs. DAC Code

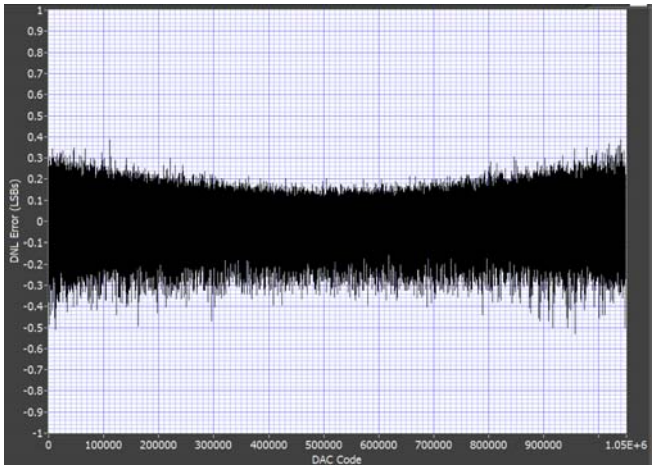

Figure 8. Differential Non Linearity Error vs. DAC Code

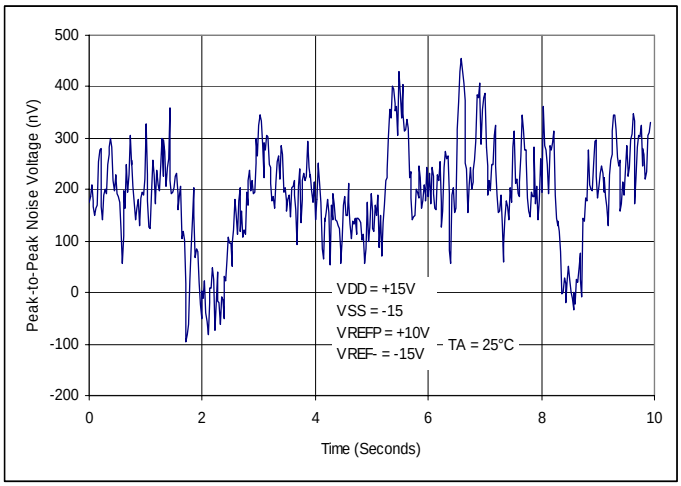

Figure 9. 0.1 Hz to 10Hz peak-to-peak Noise

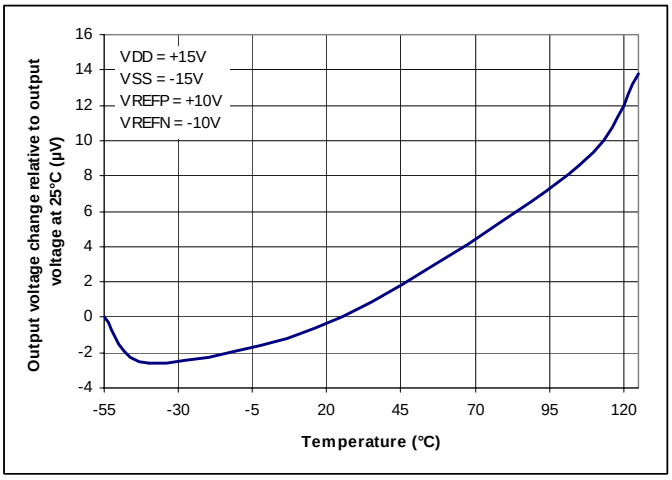

Figure 10. Output voltage Drift vs. Temperature

THEORY OF OPERATION

The AD5791 is a high accuracy, fast settling, single, 20-bit, serial input, voltage-output DAC. It operates from a V_{DD} supply voltage of 7.5 V to 16.5V and a V_{SS} supply of -16.5V to -2.5V. Data is written to the AD5791 in a 24-bit word format via a 3-wire serial interface.The AD5791 incorporates a power-on reset circuit that ensures the DAC output powers up to 0V with the V_{OUT} pin clamped to AGND through a ~6kΩ internal resistor.

DAC ARCHITECTURE

The architecture of the AD5791 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 11. The six MSBs of the 20-bit data-word are decoded to drive 63 switches, E0 to E62. Each of these switches connects one of 63 matched resistors to either the V_{REFP} or V_{REFN} voltage. The remaining 14 bits of the data-word drive Switches S0 to S13 of a 14-bit voltage mode R-2R ladder network. To ensure performance to specification, the reference inputs must be force sensed with external amplifiers.

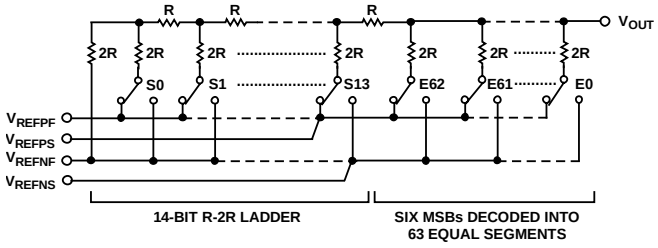

Figure 11. DAC Ladder Structure

SERIAL INTERFACE

The AD5791 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and SDIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as most DSPs. (See Figure 2 for a timing diagram.)

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK, which can operate at up to 50MHz. The input register consists of a R/$\overline{W}$ bit, three address bits and twenty register data bits as shown in Table 6. The timing diagram for this operation is shown in Figure 2.

Table 6. Input Shift Register Format

MSB					LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB0**
R/$\overline{W}$	Register Address			Register Data	

Table 7. Decoding the Input Shift Register

R/$\overline{W}$	**Register Address**			**Description**
X	0	0	0	No Operation (NOP), used in readback operations
0	0	0	1	Write to DAC register
0	0	1	0	Write to CONTROL register
0	0	1	1	Write to CLEARCODE register
0	1	0	0	Write to SOFTWARE CONTROL register
1	0	0	1	Read from DAC register
1	0	1	0	Read from CONTROL register
1	0	1	1	Read from CLEARCODE register

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before $\overline{\text{SYNC}}$ is brought high again. If $\overline{\text{SYNC}}$ is brought high before the 24th falling SCLK edge, the data written is invalid. If more than 24 falling SCLK edges are applied before $\overline{\text{SYNC}}$ is brought high, the input data is also invalid. The input register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. For another serial transfer to take place, $\overline{\text{SYNC}}$ must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register.
Once the write cycle is complete, the output can be updated by taking $\overline{\text{LDAC}}$ low while SYNC is high.

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy chain several devices together. Daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal $24 \times N$, where N is the total number of AD5791 devices in the chain. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be a continuous or a gated clock.
A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

Readback

The contents of all the on-chip registers can be readback via the SDO pin, Table 7 outlines how the registers are decoded. After a register has been addressed for a read the next 24 clock cycles will clock the data out on the SDO pin. For a read of a single register the No Operation function can be used to clock out the data, alternatively if more than one register is to be read, the data of the first register to be addressed can be clocked out at the same time the second register to be read is being addressed. The SDO pin must be enabled, to complete a readback operation, the SDO pin is enabled by default.

LOAD DAC ($\overline{\text{LDAC}}$)

After data has been transferred into the input register of the DAC, there are two ways to update the DAC register and DAC output. Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, one of two update modes is selected, synchronous DAC updating or asynchronous DAC updating

Synchronous DAC Update

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the input shift register. The DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Asynchronous DAC Update

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. The DAC output is asynchronously updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ has been taken high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

ON-CHIP REGISTERS

DAC Register

Table 8 outlines how data is written to and read from the DAC register

Table 8. DAC Register

MSB					LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB0**
R/$\overline{W}$	**Register Address**			**DAC Register Data**	
R/$\overline{W}$	0	0	1	20-bits of Data	

The following equation describes the ideal transfer function of the DAC;

$$V_{OUT} = \frac{(V_{REFP} - V_{REFN}) \times D}{2^{20}} + V_{REFN}$$

Where;
V_{REFN} is the negative voltage applied at the V_{REFN} input pin.
V_{REFP} is the positive voltage applied at the V_{REFP} input pin.
D is the 20-Bit Code programmed to the DAC

Control Register

The control register controls the mode of operation of the AD5791.

Table 9. Control Register

MSB															LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19….DB11**	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
R/$\overline{W}$	**Register Address**			**Control Register Data**											
R/$\overline{W}$	0	1	0	Reserved	Reserved	LIN COMP				SDODIS	BIN/2sC	DACTRI	OPGND	RBUF	Reserved

Table 10. Control Register Functions

Function	Description
Reserved	These bits are reserved and should be programmed to zero.
RBUF	Output amplifier configuration control
	0 Internal amplifier, A1, is powered up and resistors R_{FB} and R_1 are connected in series as shown in Figure 1. This allows an external amplifier to be connected in a gain of 2 configuration. See features section for further details.
	1 (Default) Internal amplifier, A1, is powered down and resistors R_{FB} and R_1 are connected in parallel so that the resistance between the R_{FB} and INV pins is 3.4kΩ, equal to the resistance of the DAC. This allows the R_{FB} and INV pins to be used for input bias current compensation for an external unity gain amplifier.
OPGND	Output ground clamp control.
	0 DAC output clamp to ground is removed and the DAC is placed in normal mode.
	1 (Default) DAC output is clamped to ground through a ~6kΩ resistance, and the DAC is placed in tri-state mode.
DACTRI	DAC tri-state control.
	0 DAC is in normal operating mode
	1 (Default) DAC is in tri-state mode
BIN/2sC	DAC register coding select.
	0 (Default) DAC register uses 2sComplement coding
	1 DAC register uses offset binary coding
SDODIS	SDO pin enable/disable control
	0 (Default) SDO pin is enabled
	1 SDO pin is disabled (tri-state)
LIN COMP	Linearity compensation for varying reference input spans. See Features section for further details
	0 0 0 0 (Default) Reference input span up to 10V.
	1 1 0 0 Reference input span greater than 10V

Clearcode Register

The Clearcode register sets the value to which the DAC output will be set when the $\overline{CLR}$ pin or CLR bit is asserted. The output value will depend on the DAC coding that is being used, either binary or 2scomplement. Default register value is zero.

Table 11. Clearcode Register

MSB					**LSB**
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB0**
R/$\overline{W}$	**Register Address**			**Clearcode Register Data**	
R/$\overline{W}$	0	1	1	20-bits of Data	

Software Control Register

This is a write only register in which writing a '1' to a particular bit has the same effect as pulsing the corresponding pin low.

Table 12. Software Control Register

MSB								**LSB**
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB3**	**DB2**	**DB1**	**DB0**
R/$\overline{W}$	**Register Address**			**Software Control Register Data**				
0	1	0	0	Reserved		RESET	CLR	LDAC

Table 13. Software Control Register Functions

Function	Description
LDAC	Setting this bit to a '1' updates the DAC register and consequently the DAC output
CLR	Setting this bit to a '1' sets the DAC register to a user defined value (See Table 11) and updates the DAC output. The output value will depend on the DAC register coding that is being used, either binary or 2scomplement.
RESET	Setting this bit to a '1' returns the AD5791 to its power-on state.

FEATURES

POWER-ON TO 0V

The AD5791 contains a power-on reset circuit that as well as resetting all registers to zero value, controls the output voltage during power-up. Upon power-on the DAC is placed in tri-state (it's reference inputs are disconnected) and its output is clamped to ground through a ~6kΩ resistor, the DAC remains in this state until a valid write sequence is made to the DAC. This is a useful feature in applications where it is important to know the state of the DAC output while it is in the process of powering up.

CONFIGURING THE AD5791

After power-on the AD5791 must be configured to put it into normal operating mode before programming the output. To do this the control register must be programmed. The output clamp is removed by clearing the OPGND bit and the DAC is removed from tri-state by clearing the DACTRI bit. At this point the output will go to V_{REFN}, unless an alternative value is first programmed to the DAC register.

RESET FUNCTION

The AD5791 can be reset to its power-on state by two means; either by asserting the $\overline{\text{RESET}}$ pin or by utilising the software RESET control function (SeeTable 12). If the $\overline{\text{RESET}}$pin is not used, it should be hardwired to IOV_{DD}.

ASYNCHRONOUS CLEAR

The $\overline{\text{CLR}}$ pin is an active low clear that allows the output to be cleared to a user defined value. The 18-bit clear code value is programmed to the Clearcode register. It is necessary to maintain $\overline{\text{CLR}}$ low for a minimum amount of time to complete the operation (see Figure 2).When the $\overline{\text{CLR}}$ signal is returned high the output remains at the clear value until a new value is programmed to the DAC register. The output cannot be updated with a new value while the $\overline{\text{CLR}}$ pin is low. A clear operation may also be performed by setting the CLR bit in the software control register (See Table 12).

DAC OUTPUT STATE

The DAC output can be placed in one of three states,

1. Normal operation
2. Clamped to ground through 6kΩ
3. Tri-state

The OPGND and DACTRI bits of the control register select the output state.

LINEARITY COMPENSATION

The AD5791 is factory calibrated with a reference input span of 20V (V_{REFN} = -10V and V_{REFP} = +10V). Applying a smaller reference span to the AD5791 will impact the integral non linearity performance in a minor way (1 to 2 LSBs). To compensate, a value can be programmed to the LIN COMP bits of the control register. For reference input spans of less than 10V, program 0000 to the these bits, for reference input spans of greater than 10V, 1100 should be programmed to these bits. The default value of the LIN COMP bits is 0000.

OUTPUT AMPLIFIER CONFIGURATION

There are a number of different ways that an output amplifier can be connected to the AD5791, depending on the voltage references applied and the desired output voltage span.

Unity Gain Configuration

Figure 12 shows an output amplifier configured for unity gain, in this configuration the output spans from V_{REFN} to $V_{REFP.}$

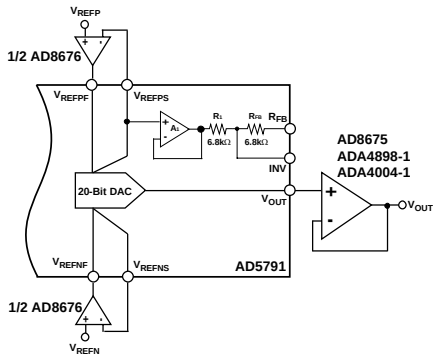

Figure 12. Output Amplifier in Unity Gain Configuration

Gain of Two Configuration

Figure 13 shows an output amplifier configured for a gain of two, the gain is set by the internal matched 6.8kΩ resistors. In this configuration the output spans from $2*V_{REFN}$ - V_{REFP} to $2*V_{REFP}$ - $V_{REFP.}$ This configuration is used to generate a bipolar output span from a single ended reference input, i.e. with V_{REFN} = 0V. For this mode of operation the RBUF bit of the control register must be cleared to logic 0.

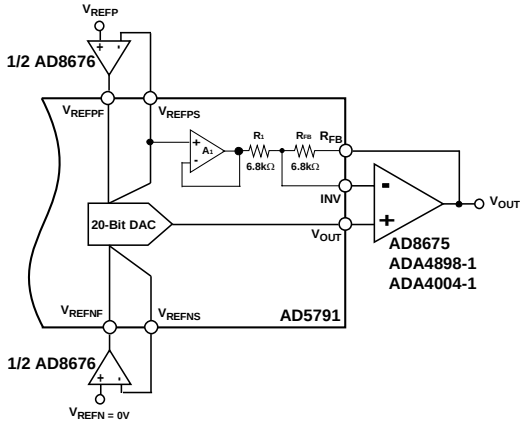

Figure 13. Output amplifier in Gain of Two Configuration

APPLICATIONS

TYPICAL OPERATING CIRCUIT

Figure 14 shows a typical operating circuit for the AD5791 using an AD8676 for reference buffers and an AD8675 as an output buffer. To meet the specified linearity, force sense buffers must be used on the reference inputs. Because the output impedance of the AD5791 is 3.4kΩ, an output buffer is required for load driving.

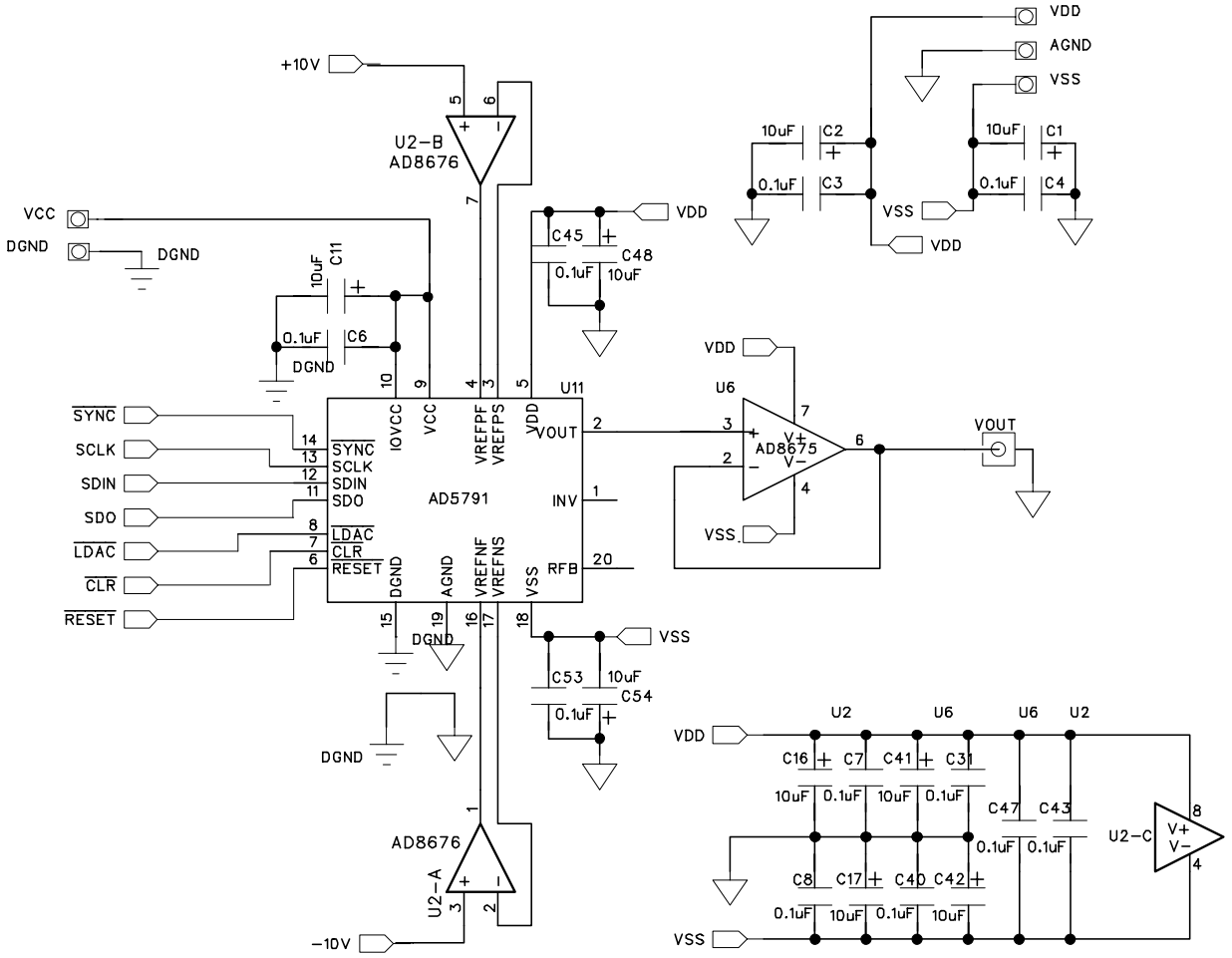

Figure 14. AD5791 Typical Operating Circuit

EVALUATION BOARD

An evaluation board is available for the AD5791 to aid designers in evaluating the high performance of the part with minimum effort. The AD5791 evaluation kit includes a populated and tested AD5791 PCB. The evaluation board interfaces to the USB port of a PC. Software is available with the evaluation board to allow the user to easily program the AD5791. The software runs on any PC that has Microsoft windows XP (SP2) or Vista (32 Bit) installed. The EVAL-AD5791 datasheet is available, which gives full details on the operation of the evaluation board.

OUTLINE DIMENSIONS

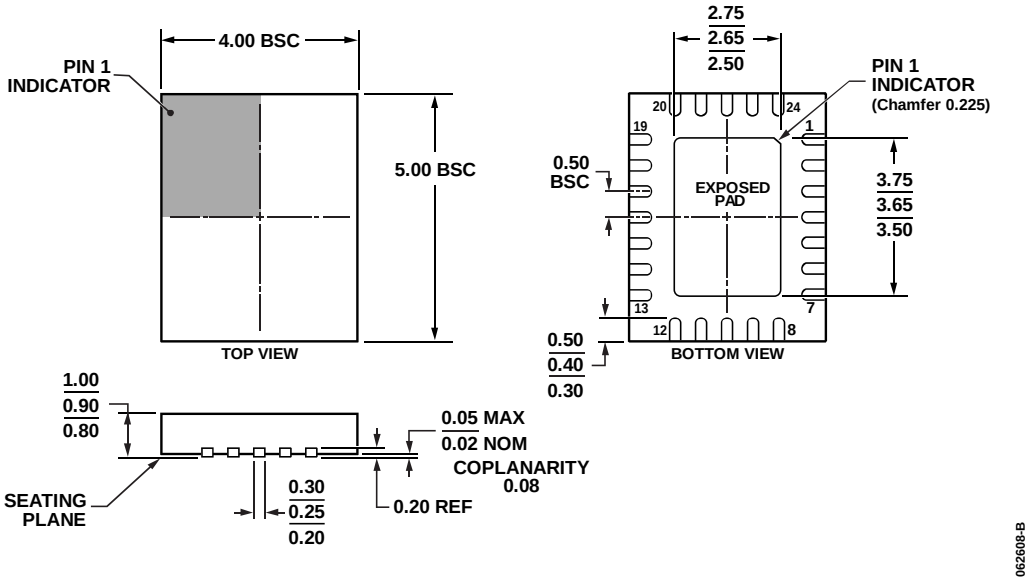

Figure 15. 24-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-24-5)
Dimensions shown in millimeters

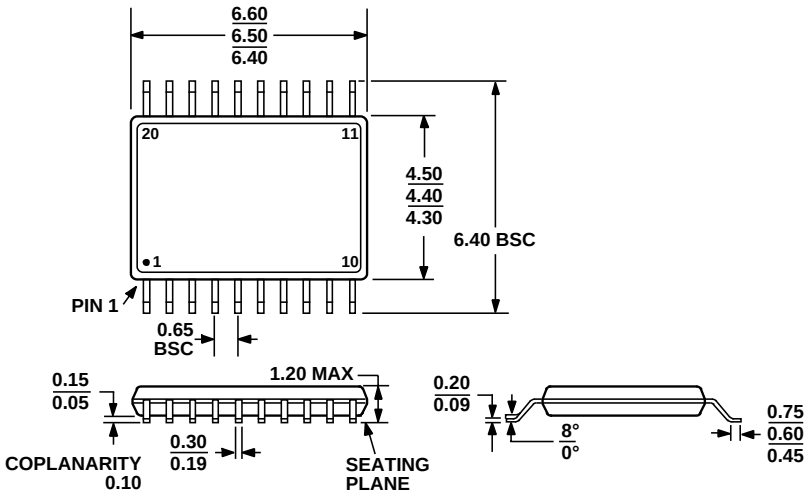

Figure 16. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	INL	Package Description	Package Option
AD5791BCPZ	−40°C to +125°C	±1LSB	24-Lead LFCSP	CP-24-5
AD5791ACPZ	−40°C to +125°C	±4LSB	24-Lead LFCSP	CP-24-5
AD5791BRUZ	−40°C to +125°C	±1LSB	20-Lead TSSOP	RU-20
AD5791ARUZ	−40°C to +125°C	±4LSB	20-Lead TSSOP	RU-20

NOTES

PR08964-0-3/10(PrG)